Delivering Package Innovations to Enable Future Products

Introducing the Industry's First 90nm - Low K Organic Flip Chip Package

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Technology Manufacturing Group

Chandler, Arizona

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Agenda

- Packaging @ Intel
- Convergence… Changing the Role of Packaging
- Packaging Challenges & Innovations Intel is Delivering
- Summary

Assembly Technology Development

ATD's main R&D facility located in Chandler, AZ

The Assembly Technology Research Lab… exploring new assembly capabilities

Our Mission - Identify, Develop an Deliver Total Interconnect Solutions to Meet Intel's Business Needs

Intel's Global Packaging Development

Distributed centers of excellence worldwide

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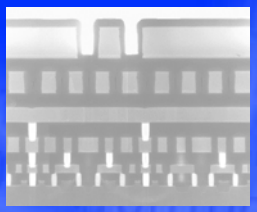
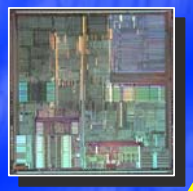
* Also Intel Assembly and Test Site

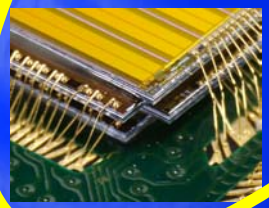
From Transistors to Systems ... Innovation in All Areas



Transistor-to-Transistor

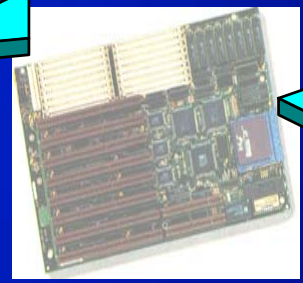


Chip-to-Package



Our Goal

Innovative, Efficient, High Performance, Low-cost Packages that Gives Intel Silicon a Significant Competitive Advantage



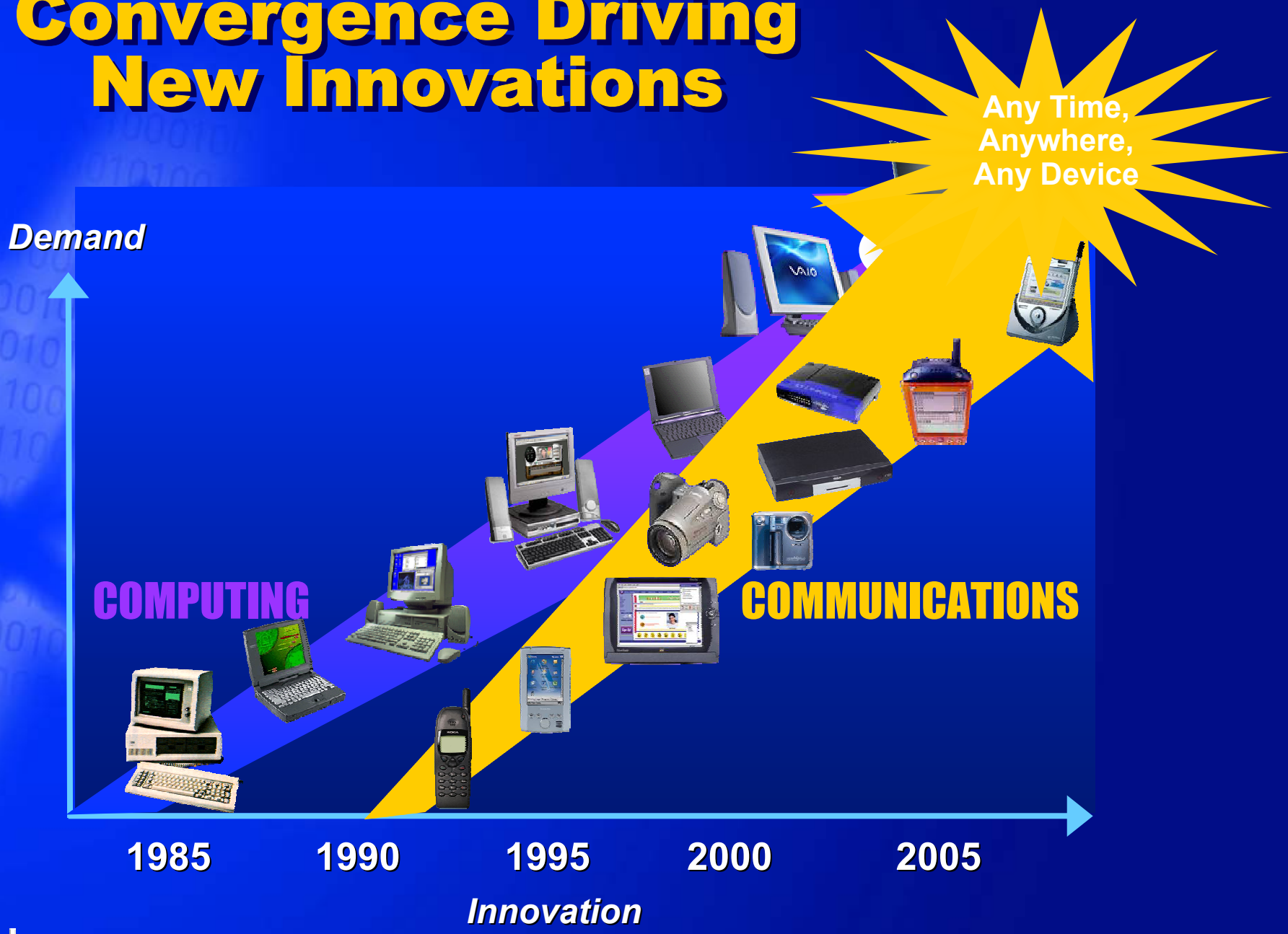
Package-to-Board

Board-to-System

Key Element

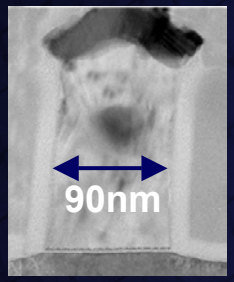
Convergence… Changing the Role of Packaging

Convergence Driving New Innovations

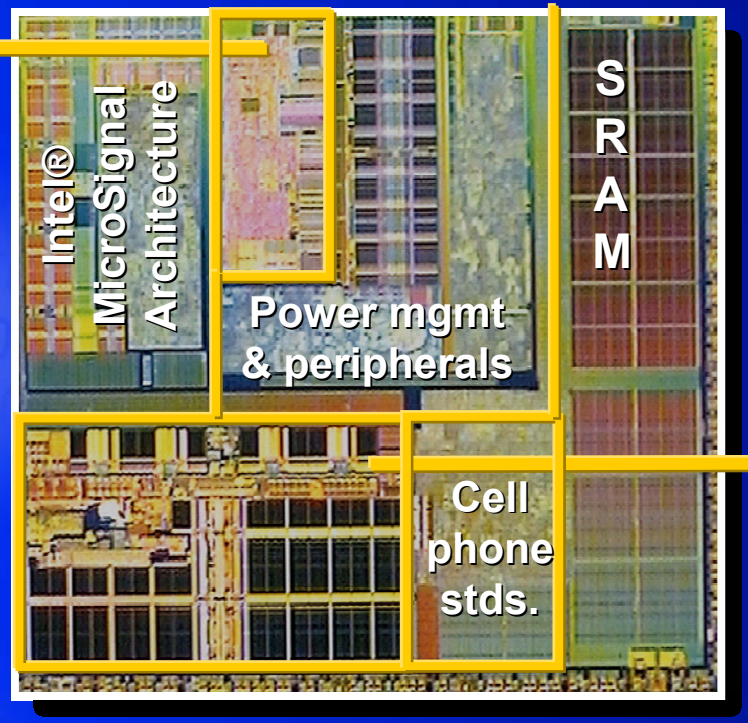


Integration via Silicon (SoC)

Logic

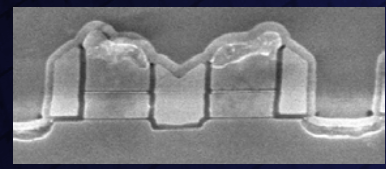


90nm Transistor Gate on 0.13µm Process



Flash+Logic

Flash

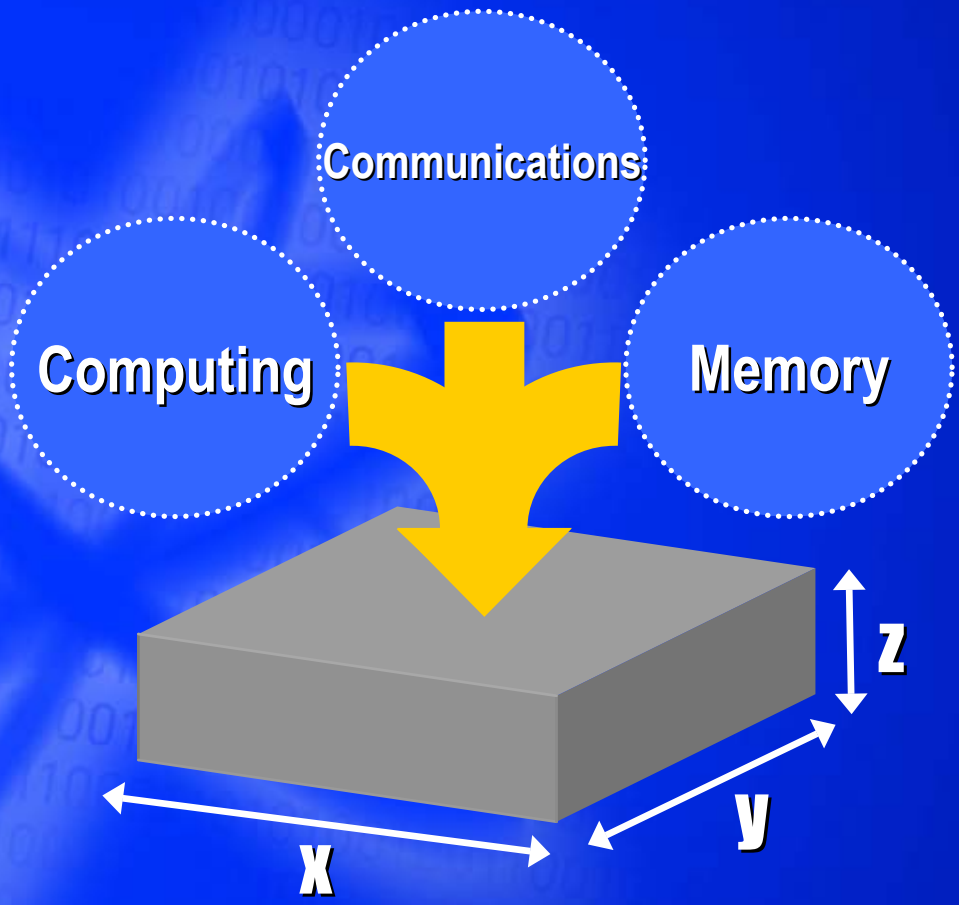


0.16µm² Flash Cell

Density, Speed, & Power Consumption are Increasing… Packaging Must Adapt to Manage Integration of New Features

Source: Intel

Converged Devices Require
Mips & Mbit / milliwatt & millimeter^3



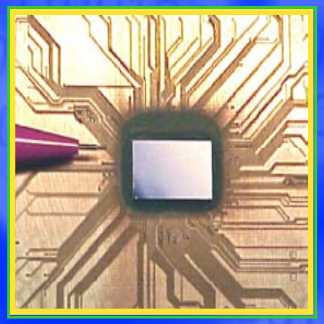
- Combination of stacking and integration required
  - x, y, z dimensions shrinking
- Bigger “M’s” and smaller “m’s” are better

Convergence Increases Silicon Usage and Need for System in Package Solutions

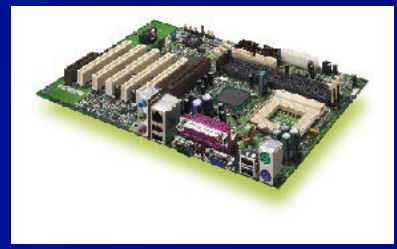
The Solution… Intel Brings it all Together

Packages

Silicon



Motherboard



- Architectural Changes to Silicon Design
- Enhance Package / Substrates
- Enabling Technology on Motherboards
- Novel Cooling & Power Delivery Solutions
- System Integration & Enabling

Power Delivery & Heat Removal

Systems

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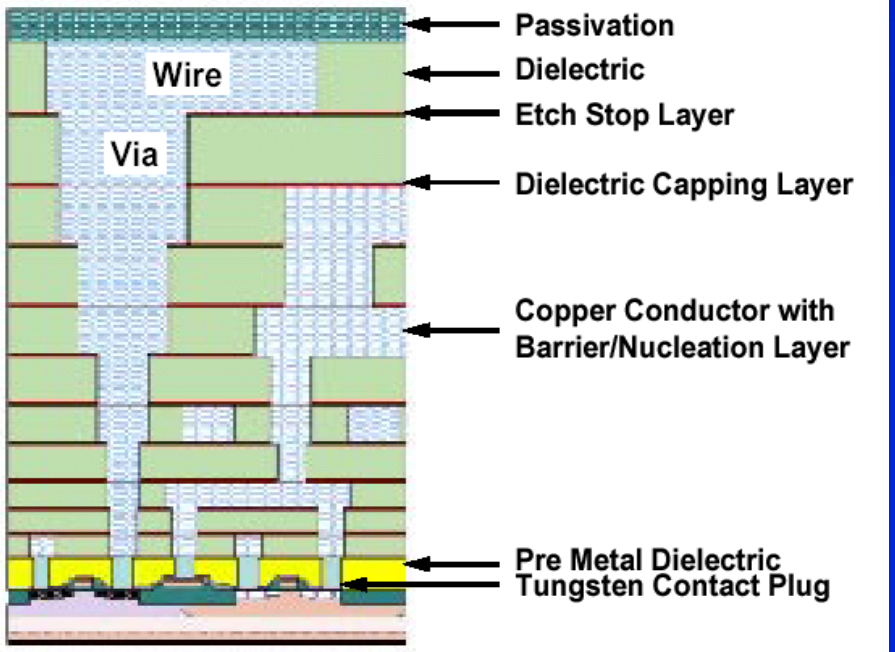
Packaging Challenges & Innovations Intel is Delivering

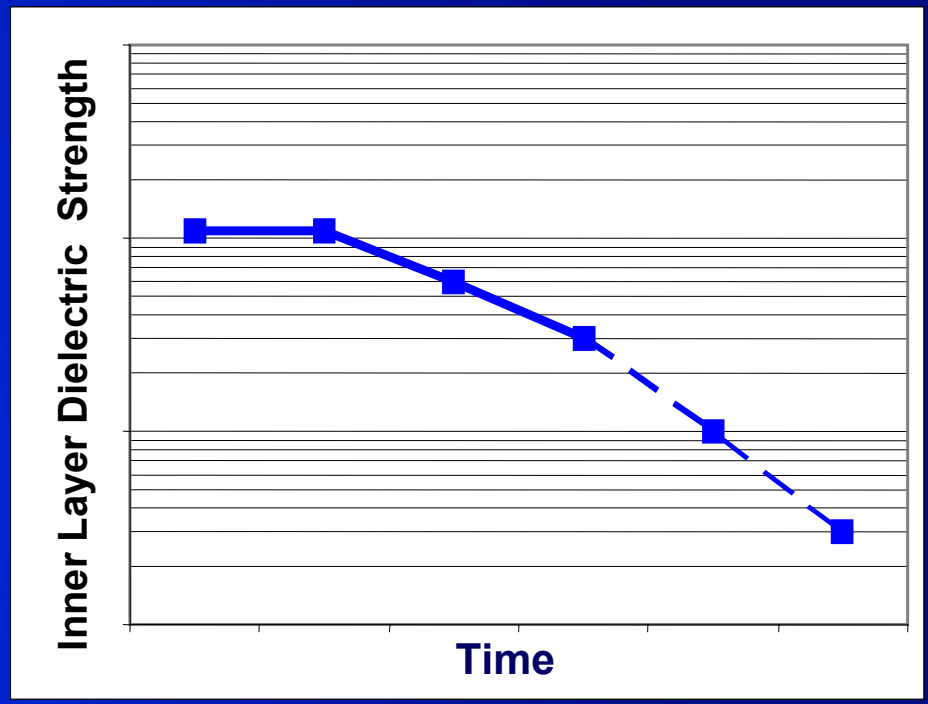
Packaging Challenges

1. Industry Silicon & Package integration becomes more complex at 90nm and beyond
2. Cooling complexity increases
3. Interconnect scaling needs novel approaches to enable new product features
4. Chip Scale Packaging - System-in-a-package
5. The Road to Lead free

Goal : Bring technology innovation into High Volume Assembly at a Low Cost

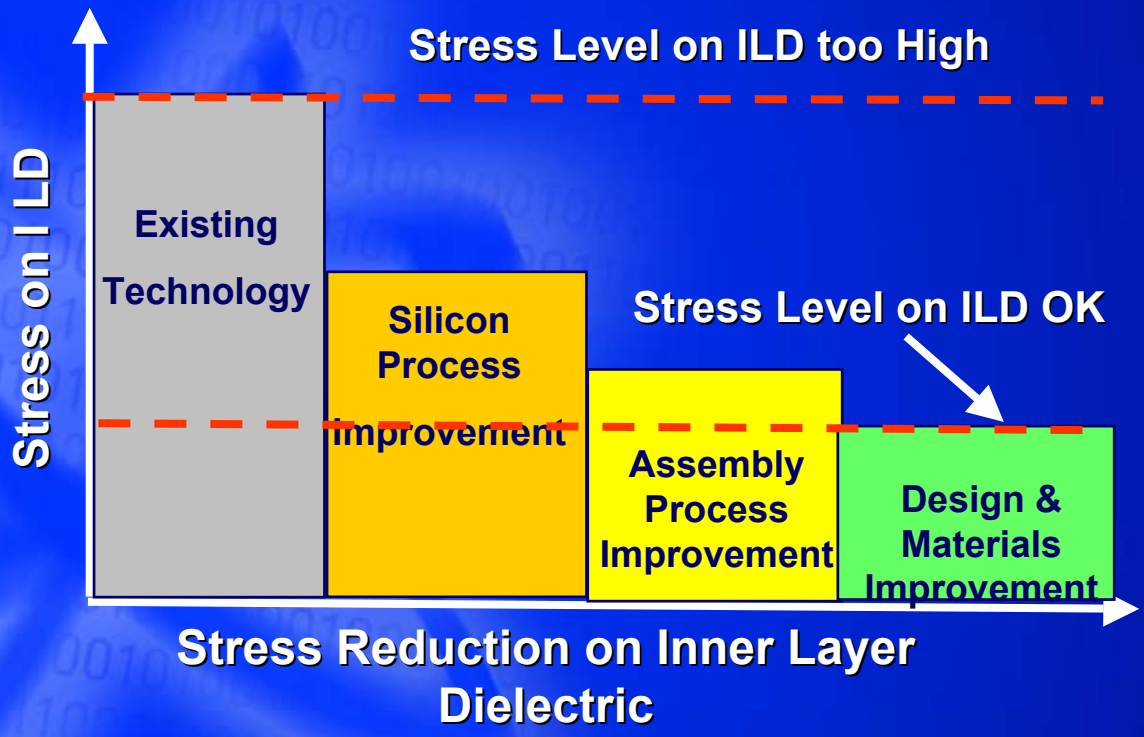
Silicon & Package Integration More Complex

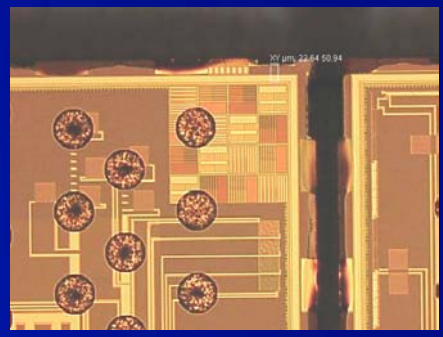




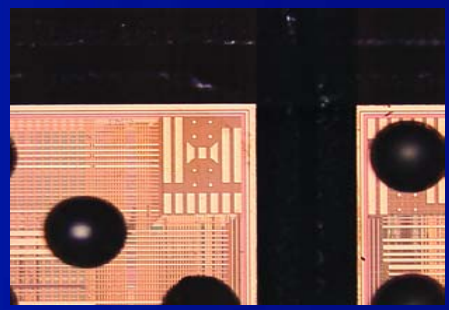
- The Industry Challenge
  - Circuit Signal Speed is impacted as silicon feature sizes are reduced (delay is proportional to 1/RC)
  - Transition to Lower K dielectric materials is required to reduce capacitance (charging delays)
- Successful Integration of Low K Dielectric Material into Silicon & Flip Chip Package Technologies requires a significant reduction in Inner Layer Dielectric Stress (ILD)

Silicon & Package Integration Solutions





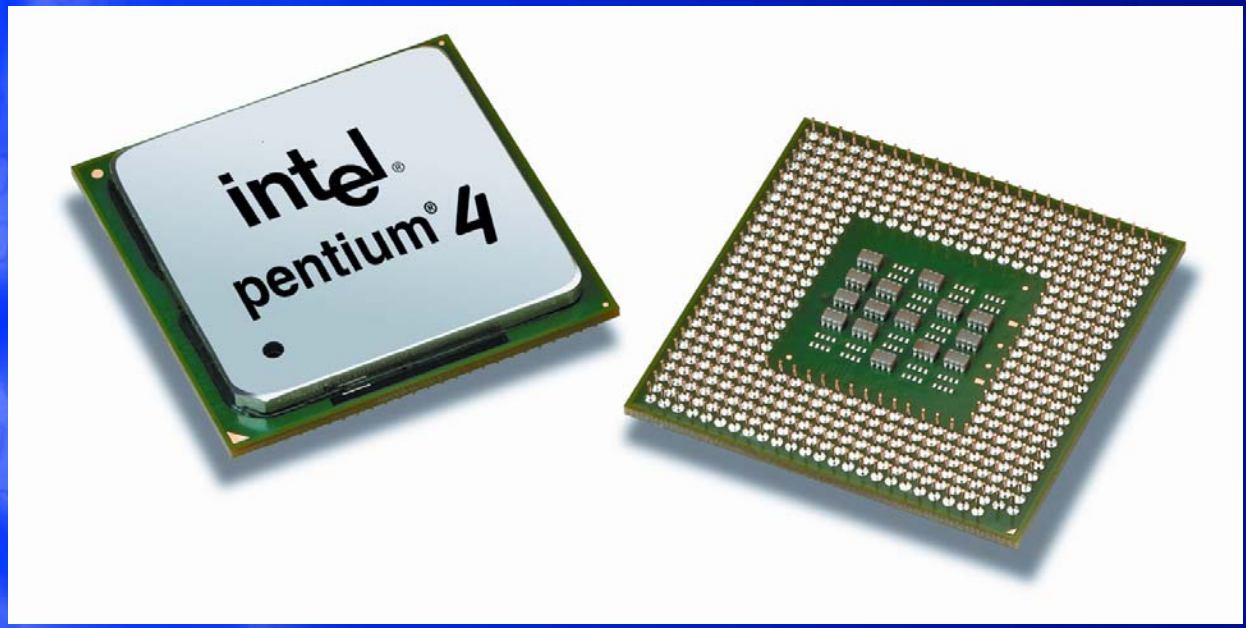
Existing Process



New Process

Intel's Assembly Technology Development Capabilities Enable Understanding and Integration of All Design, Process and Materials Aspects

Introducing the Industry's First 90nm Low K Organic Flip Chip Package



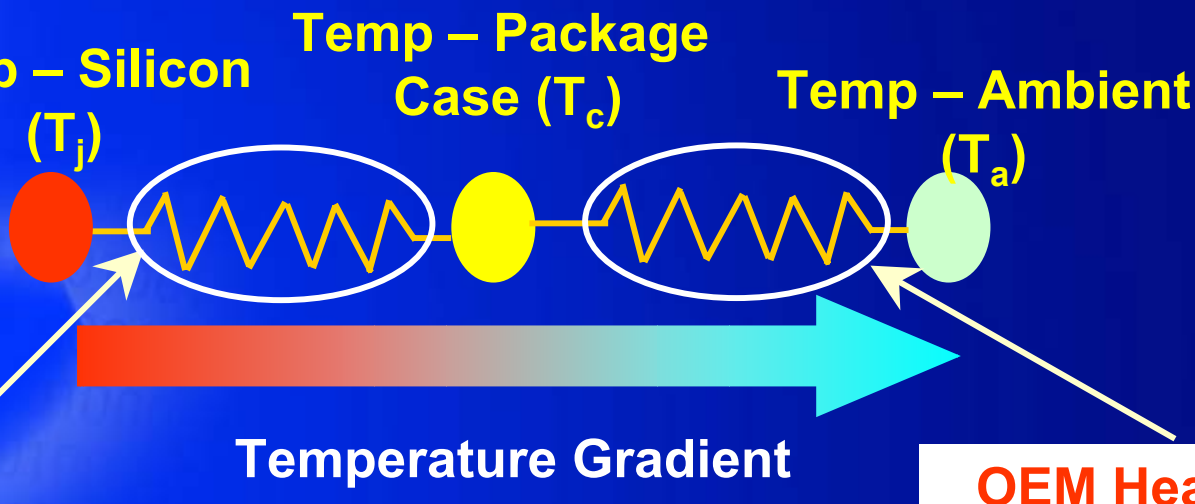
WE ARE NOW SAMPLING on 90nm Technology

Packaging Challenges

1. Industry Silicon & Package integration becomes more complex at 90nm and beyond
2. **Cooling complexity increases**
3. Interconnect scaling needs novel approaches
4. Chip Scale Packaging - System-in-a-package
5. The Road to Lead free

Cooling

Total Package + System Solution Thermal Budget

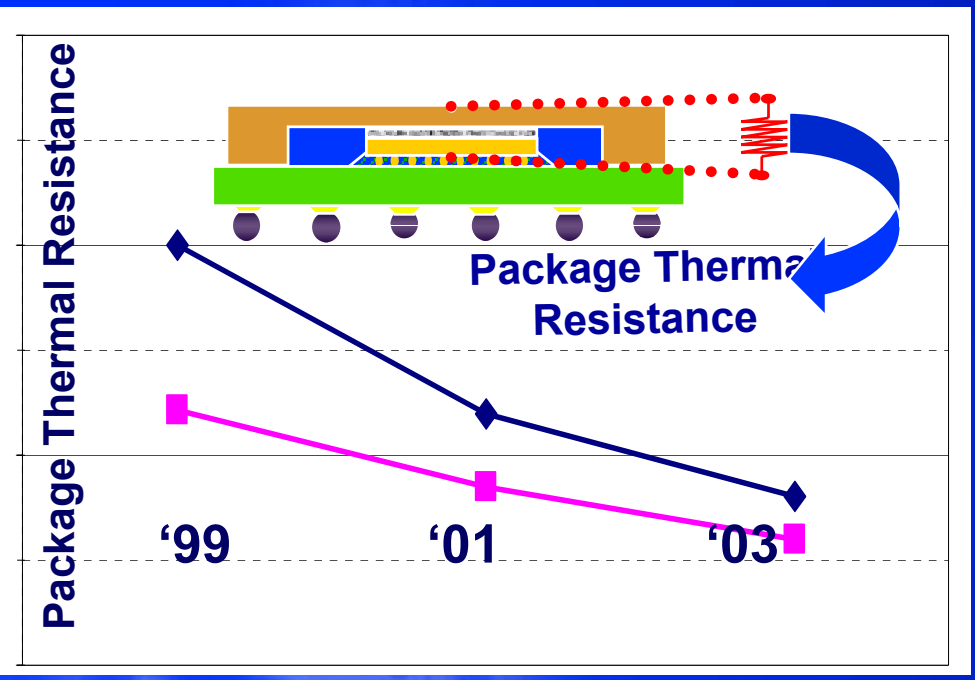


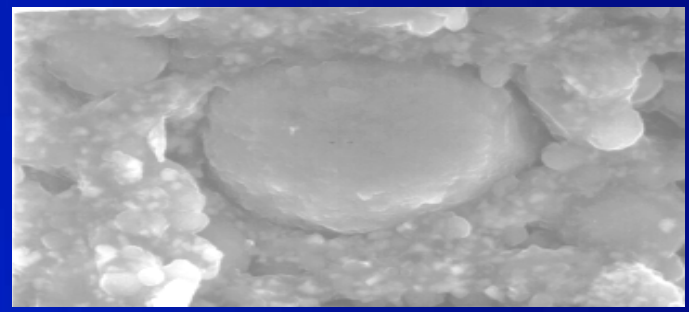
Packaging
Provide Solutions
for this interface
of the budget :
Smooth out Hot Spots

OEM Heat Sink
Provide Solutions
for this interface
of the budget

Integrated Thermal Solutions In The Package
Reduce Heat Flux – Easier To Cool In The System

Cooling Complexity Increases



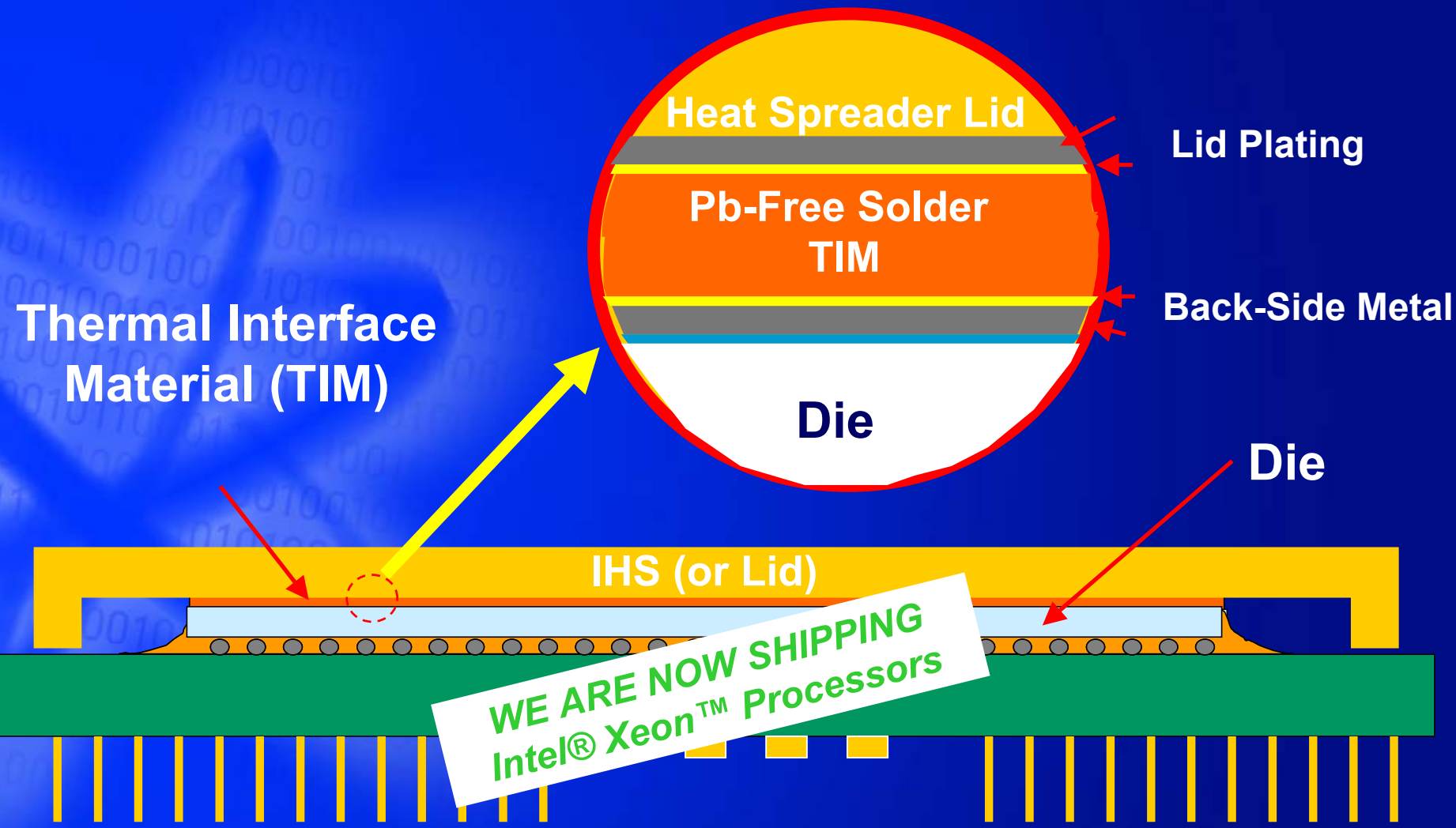


Adjusting Material Formulation (filler size, loading, distribution) to Improve Thermal Conductivity

Continuing to Reduce Thermal Resistance by Optimizing Polymer Interface Material Fillers is an Industry Challenge

Intel Focused On Fundamental Materials Formulation Research & Reducing Process Variability

Solder Thermal Interface Material

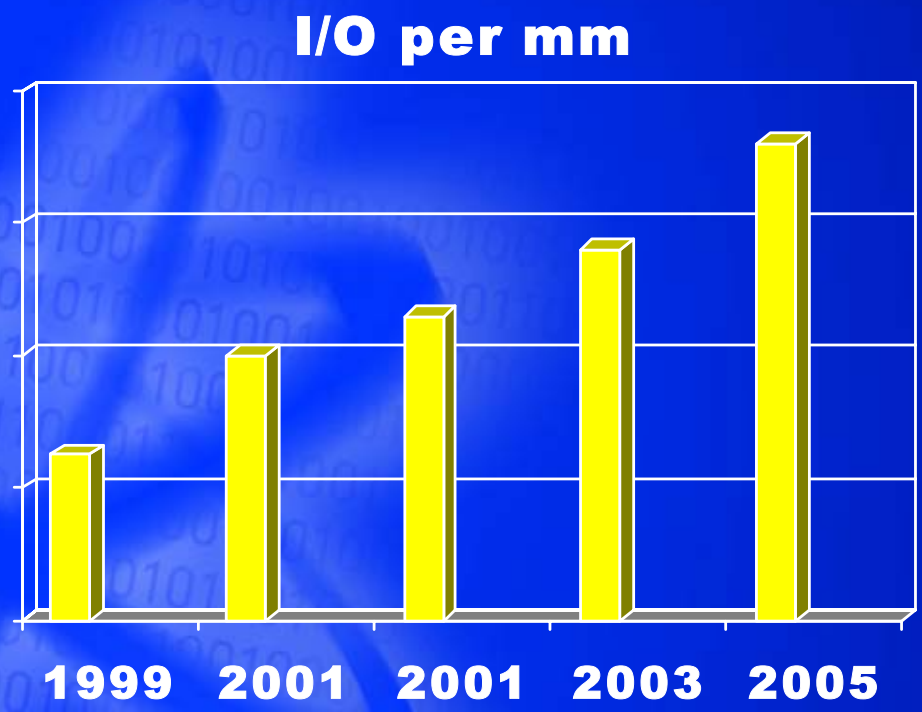


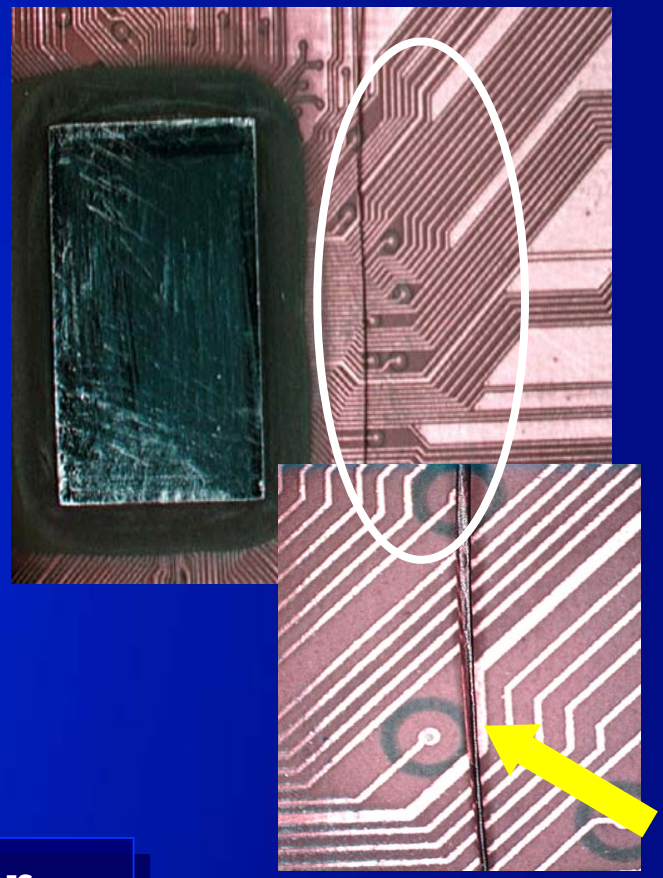
Introducing – Industry's First High Volume Solder Thermal Interface Material Process on Organic Packaging

Packaging Challenges

1. Industry Silicon & Package integration becomes more complex at 90nm and beyond
2. Cooling Complexity Increases
3. **Interconnect scaling needs novel approaches to enable new product features**
4. Chip Scale Packaging - System-in-a-package
5. The Road to Lead free

Package Interconnect Scaling

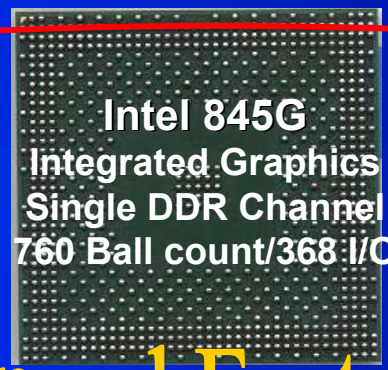




Lines ~ 1/3 width of human hair (60um)

New Features Drive Higher Wiring Density

Package Interconnect Scaling



WE ARE NOW SHIPPING
Intel 865G & 875P Chipsets

Enhanced Feature Set

Flip Chip BGA
1.27 mm solder ball pitch

1.00 mm solder ball pitch
Increased I/O Capability
28% Increase!

'Balls Anywhere' Pattern
& Advanced Routing Design
Increased I/O Capability 44%!

Intel Maintained Constant 37.5 mm Package Size while Increasing Features

Enhancing Product Features While Maintaining Packaging and Motherboard Technology Cost Structure

Packaging Challenges

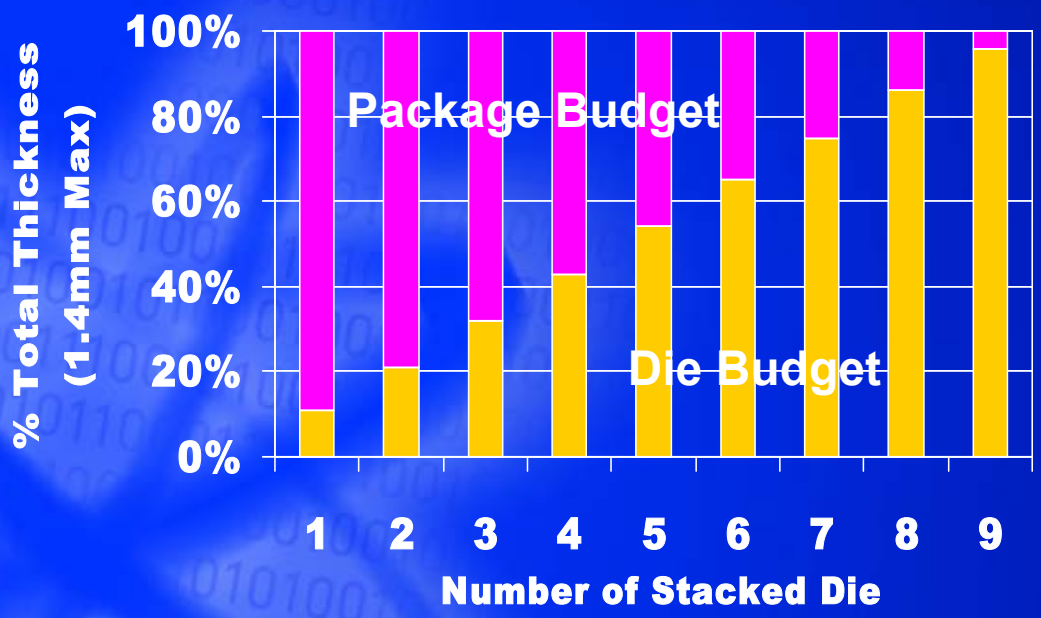
1. Industry Silicon & Package integration becomes more complex at 90nm and beyond
2. Cooling complexity increases
3. Interconnect scaling needs novel approaches
4. **Chip Scale Packaging - System-in-a-package**
5. The Road to Lead free

Chip Scale Packaging Trends

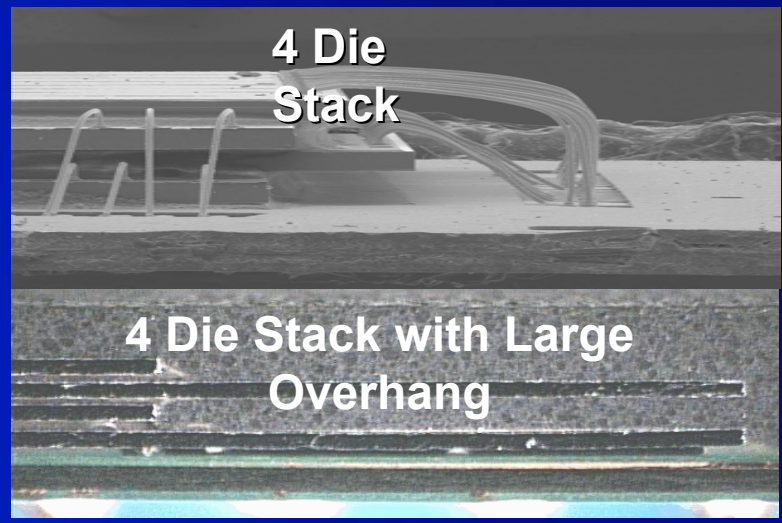
- Chip Scale Package Pitch Reduction to .5mm (for those ready)
- Memory and System in Package
  - Stacked Die and Stacked Pac
    - Last year we sai
    - Nov
    - Die, Went to 3 Die, Going to 4,5,6 Die
  - , thin, thin
    - 2002 was .150 mm die
    - Now Sampling in .075 mm die
    - Tomorrow…. Less than that

Greater Performance, Memory, Computing in smaller mm^3 space

Integration via Packaging - Thinning & Stacking



Thin Die Enables Thinner Packages



But Challenges to Handling, Bonding, & Stacking

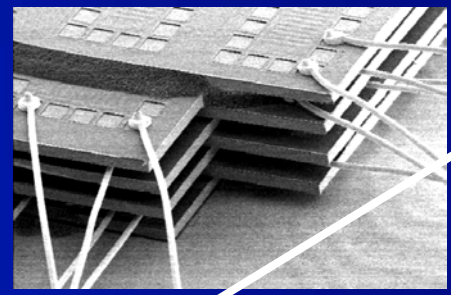
Die Thinning and Stacking is Critical to Achieve SIP

Intel has Developed Assembly Processes to Reduce Overall Die and Package Thickness

Introducing Ultra-Thin Packaging (Intel® UT-SCSP)

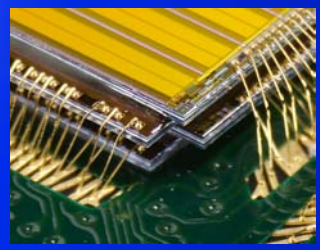
- Extending the envelope with more die in less space
- 4 to 5 Die in 1mm to 1.2 mm Package Height
- High Volume Capability with High Reliability

Ongoing Research



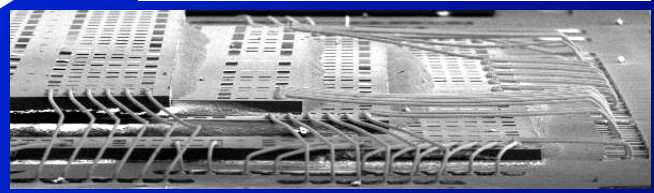
8 Die Stack
50 µm Die

Intel® UT-SCSP

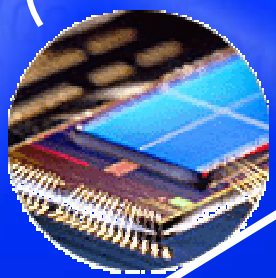


4 to 5 Die
1 to 1.2 mm

75 µm Die Thinness



>150 M Units Shipped



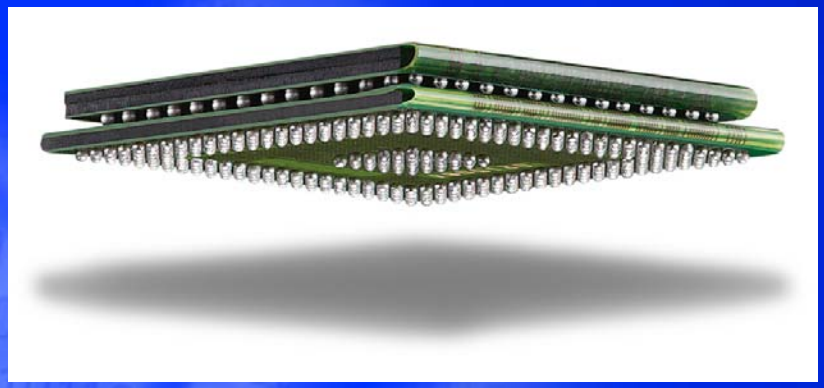
2 to 3 Die
1.2mm

125 - 175 µm Die Thickness

2 Die
1.4mm Package Height

The Ultimate Flexibility

Introducing Intel® Folded Stacked Chip Scale Package

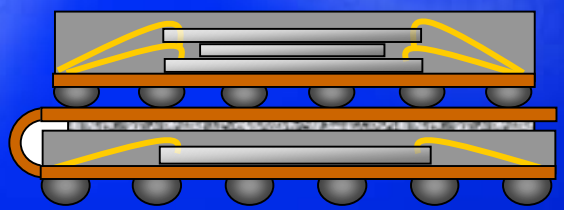


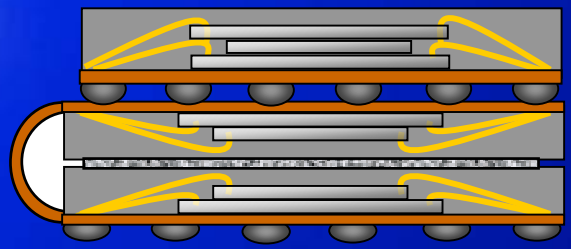
Industry's First !! - Intel® Folded Stacked Chip Scale Package
A system in Package

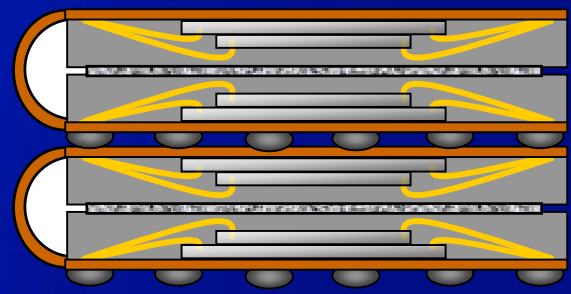
We Announced in 2002 that We Would Be Sampling

WE ARE NOW SAMPLING

Many Configurations of Logic & Memory Possible





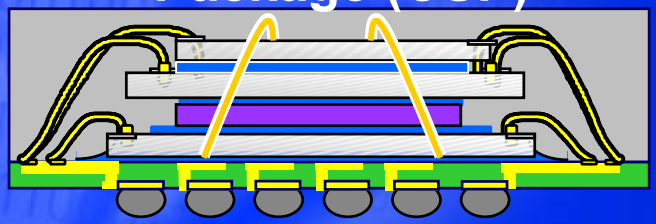


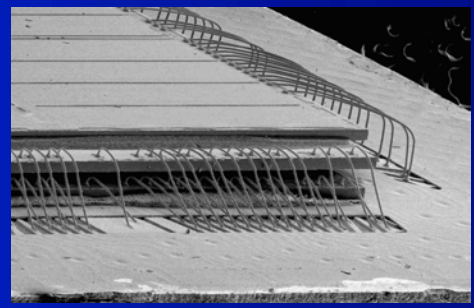
Logic - Memory System-in-a-Package
Several Flavors Being Developed

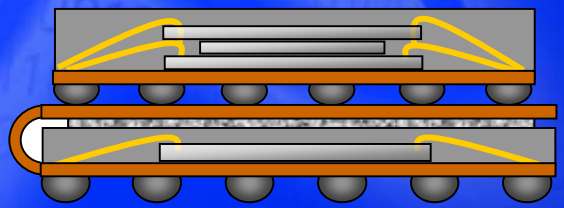
SHIPPING

PXA261, PXA262, PXA263

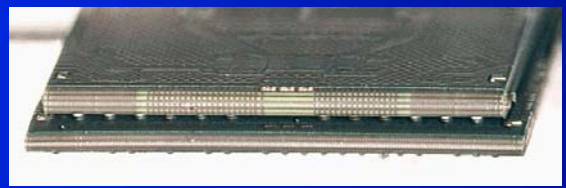
Intel® Stacked Chip Scale Package (CSP)







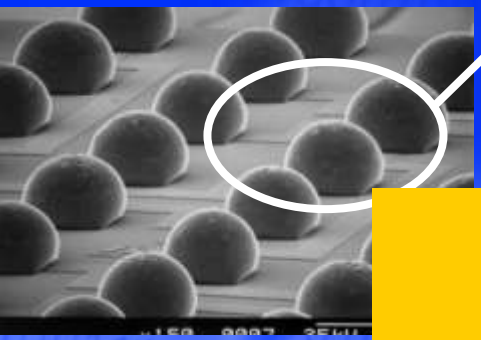
Intel® Folded-SCSP



SAMPLING

Flip Chip in CSPs

Array of Flip Chip Bumps on Chip

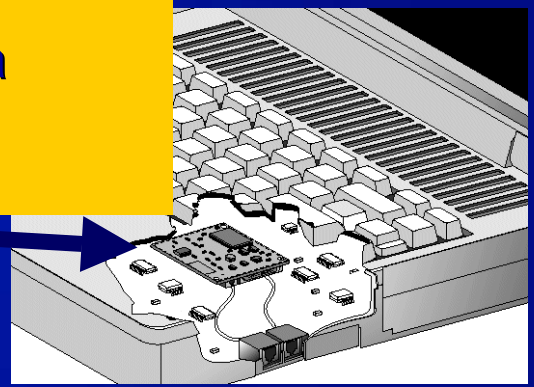


FC-CSP wit
Exposed Di

Flip Chip Enables

- Higher frequencies and R/F performance
- Reduction in package body size
- Higher I/O in smaller chip area

h
ip CSP



Packaging Challenges

1. Industry Silicon & Package integration becomes more complex at 90nm and beyond
2. Cooling complexity increases
3. Interconnect scaling needs novel approaches
4. Wireless packaging - System-in-a-package
5. **The Road to Lead free**

Industry Pb-free Challenges

- Reliability of Pb-free Solutions Across Industry at Elevated Temperature
  - Capable at Pb-free Board Process Temp. (260C Pb-free vs 220C SnPb)
  - Compatibility of multiple solders in sub-components in Pb-free board process
- Pb-free Industry Infrastructure Readiness
  - Supply chain readiness →100% BOM availability
  - Availability/ HVM capacity of Pb-free components and materials
  - Management of conversion logistics and dual-line (Pb and Pb-free)
- Pb-free Platform Cost

Intel is Committed to Finding Appropriate and Cost-Effective Ways to Reduce Lead in its Products

The Road to Pb-Free

- Several Pb-free products are available and shipping today
  - Intel certified its first Pb-free product in October 2001 and shipped its first Pb-free product October 2002
  - Packages include: Very Thin Profile Fine Pitch BGA (VF BGA), Intel® Stacked Chip Scale Package , P-BGA
- Pb-free Second Level Interconnect development for Flip-Chip Packaging technology is underway
  - Focused on newer technologies under development
- Reduction of Hazardous Substances (RoHS) compliant product introductions will occur in phases

Summary

Summary

- **Many Challenges are Being Met…**
  - Silicon/Package Integration… Transition to new dielectric materials
  - Cooling Complexity… New products require better Interface Materials
  - Interconnect Scaling… New features require more interconnect
  - System in Package… Thinner Die and Packages
  - Road to Lead Free… Intel is committed to the Industry Challenge

Intel's Integrated Design, Silicon, Packaging Technology Development Enable the Delivery of Optimized Solutions into High Volume

Thank You !

For more information, please visit ….

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